CDC – Configurable Display Controller IP block

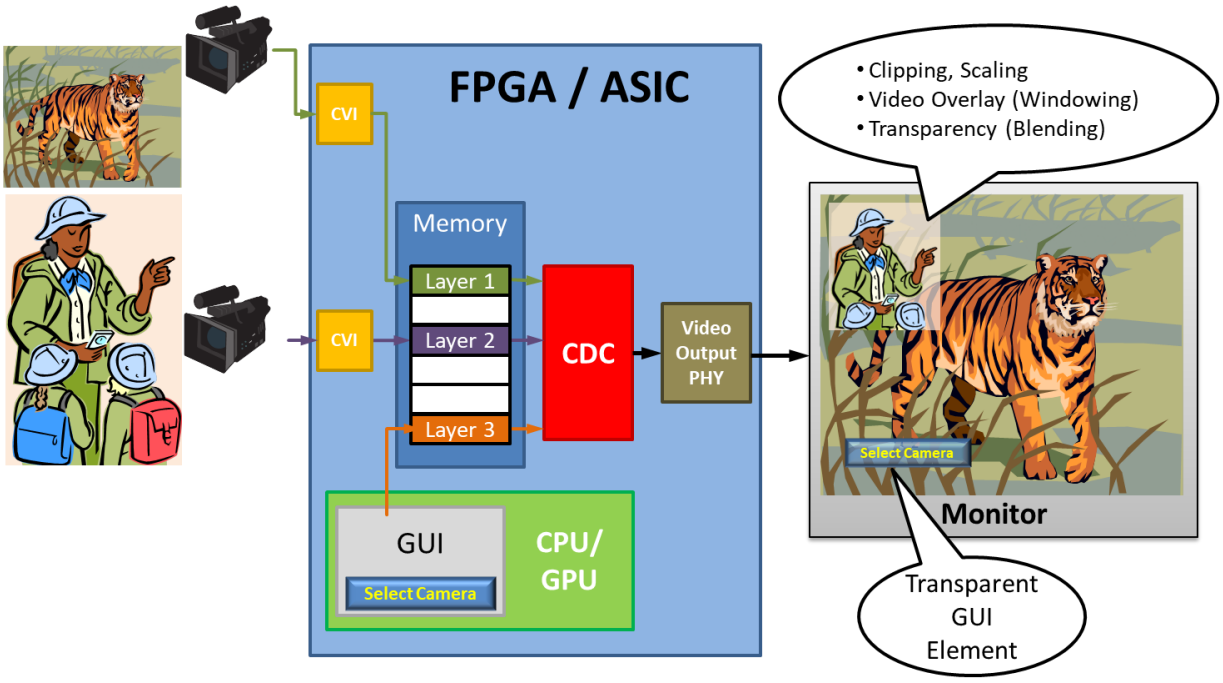
Product Brief

Overview

CDC is a fully **C**ustomizable **D**isplay **C**ontroller IP supporting the OpenWF display API specification. A number of features can be configured at synthesis time and programmed at run time. The display controller can be applied to e.g. FPGA systems with a resource optimized, application specific feature configuration or to ASIC projects applying a more generic feature set and thus more flexibility.

The main functionality of **CDC** is reading images (layers) from memory, combining them on-the-fly e.g. by blending, cropping and windowing and generating a video output stream of the combined image.
On the output the controller provides a digital RGB signal with video data and signals for horizontal/vertical blank and synchronization. Optionally a digital component (YC_BC_R) output signal can be configured at synthesis time. The **CDC**'s output typically is then connected with the physical display output block like an HDMI our LVDS IP block or a Video DAC.

Application Example



In this example, images from two video cameras are transferred to frame buffers in memory using two CVIs (**C**onfigurable **V**ideo **I**nput controller, another TES IP), while the internal

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CPU/GPU generates GUI elements to be used in the displayed image in a 3rd framebuffer. The **CDC** clips and scales the image stored in layer 2 and blends it with the main image on layer 1, using windowing to display it in the upper left corner, while adding some transparency to keep the occupied part of the main image visible. The GUI element is blended into the lower left corner, again using the transparency feature of the **CDC**.
The resulting image is transferred to a Video PHY block, which provides a standard video display interface (e.g. SVGA, DVI, HDMI) suitable for the attached monitor.

CDC Configurability

Based on a highly modular architecture the **CDC**-Family (**CDC-200**,**-300**,**-400**,**-500**) offers a wide range of features from **CDC-200** providing basic functionality with each family member offering additional configurable feature extensions up to the flag-ship **CDC-500** which supports output image rotation.

The target set of features is configurable at synthesis time, resulting in an optimally tailored solution for the target application: not needed features and the related modules are not synthesized, resulting in less resource usage (FPGA logic elements or ASIC gates) and power consumption.
The most important features that can be customized are the usable color formats, number of input layers, scaling option, rotation and blending. The maximum number of (A)RGB/YC_BC_R layers is only dependent on the bus bandwidth and timing constraints.

The selected (configured) features can be controlled at run-time via software-programmable registers. To ease the application programmers' life an ANSI-C software driver is delivered providing a set of comfort functions.

General CDC Features

These features are included in every member of the **CDC**-family (**CDC-200**,**-300**,**-400**,**-500**).

- High Resolutions
  - Up to 64k x 64k pixels
  - Maximum resolution can be constrained at synthesis time to save resources
  - Programmable resolution needs external programmable PLL

- Multiple Layers
  - Number of layers and layer-specific features configurable at synthesis time
  - Blending
    - Layer blending
      - $color_{Result} = f_n \times color_n + f_{n-1} \times color_{n-1}$; n: layer position
    - Blending technique configurable at synthesis time:
      - Simplified algorithm (less gates/LEs)
      - Precise algorithm (more gates/LEs)
    - Blending modes for each layer, configurable at synthesis time
      - Standard alpha blending
      - Pre-multiplied alpha layers

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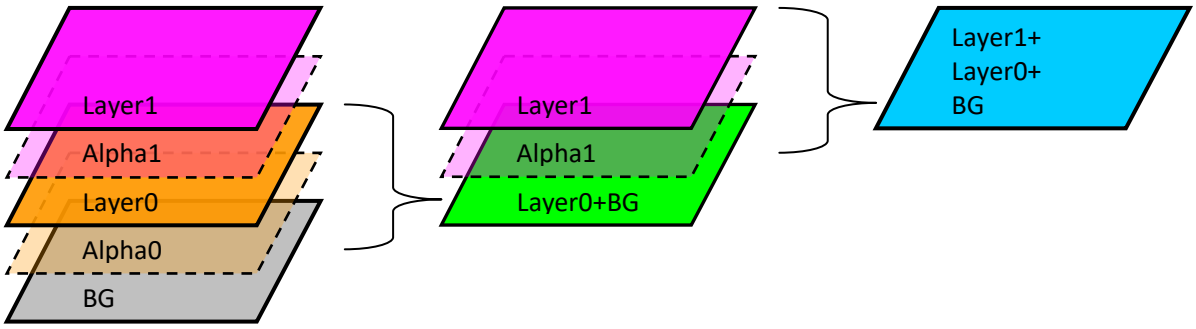
        - Additional constant alpha (fade in/out of layers)
    - Per-pixel alpha can be stored in dedicated alpha layers (8 bit alpha)
    - Configurable background layer for multi-color backgrounds (needs extra internal memory) or single programmable background color



- Windowing
    - Blending only a programmable rectangular area of one layer into the other
        - 'Picture-in-Picture' video overlay
        - Multiple still images and videos on one display

- CLUT (Color Look-Up Table) option for every layer
    - Usage of indexed formats, e.g.
        - 8 bit indexed
        - 8 bit alpha + 8 bit indexed
        - 4 bit alpha + 4 bit indexed
    - Up to 256 24 bit color values in CLUT RAM

- Color Keying
    - Define transparent color for formats without alpha

- Gamma Correction
    - Adapt image output to display characteristics
    - Brightness + contrast control

- Dithering
    - Softer color transitions for displays with less color depth
    - Flexible dithering: switched on and off during run-time
    - Different implementations selectable (trade-off flexibility vs. resource usage)
        - Ordered dithering
        - Pseudo random dithering

- Flexible Input Color Formats
    - Up to 8 input formats selectable per layer
    - Available input color formats :
        - 32 bit ARGB8888
        - 24 bit RGB888
        - 16 bit RGB565
        - 16 bit ARGB1555

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        - 16 bit ARGB4444
        - 8 bit luminance, no alpha
        - 8 bit alpha/luminance 44
        - 16 bit alpha/luminance 88
    - Available output color formats:
        - RGB 888
    - Internal pixel color format is ARGB8888

- Parallel Pixel Output
    - RGB888 (24 bit)
    - Pixel clock, HSync, VSync, Data enable (polarity configurable)
    - Serialization logic (e.g. OpenLDI, MIPI DSI) can easily be adapted

- Dual-View and Dual-Port Modes
    - Assign layers to two independent views/ports
    - Support of special dual-view panels
    - Support of dual-link modes

- Slave Timing Mode
    - Input synchronization to external video source timing instead of internal timing generator

- Bus system
    - Generic bus interface easily adaptable to any target bus system
    - **CDC** currently supports AMBA APB and AHB/AXI4 as well as the IntelPSG (ex. Altera) Avalon bus interface.

CDC-300 Extensions

- Image Scaling
    - Bilinear scaling (up- or downscaling) allows independent sizes for input and output images
    - Individual scaling of every input layer
    - Availability of scaler can be configured at synthesis time per layer

- Horizontal and Vertical Image Mirroring

- Additional Input Color Formats: Individual layers may be configured at synthesis time to accept digital component signals (YC_BC_R) of the following formats:
    - YC_BC_R 4:2:0 fully/semi planar
    - YC_BC_R 4:2:2 interleaved

CDC-400 Extensions

- Additional YC_BC_R Input Color Formats
    - YV12
    - I420

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- Digital Component Signal Output option configurable at synthesis time
  - Output format: YC_BC_R 4:2:2 (16 bpp)
  - The coefficient set for YC_BC_R calculations can be selected at run time from a set of two configurable (ST) coefficient sets, for example ITU-R BT.601 and ITU-R BT.709.
  - Selectable C_B/C_R order

- Flexible Layer Blending Order
  - Instead of a fixed blending order (see **CDC-200**), a custom blending order is programmable at runtime.

- Viewer-Friendly Missed-Pixel Handling
  - Display of last valid pixel in case of next pixel data not arriving in time due to bus overload
  - Avoids display of undefined pixels (noise)

- Single Frame Mode
  - Display a single frame when triggered (either software or hardware trigger)
  - Support for displays with internal frame buffer

- Dual CPU Support
  - Configurable secondary interrupt register to enable individual IRQ handling for each CPU
  - Memory and address bus access needs to be handled by an external arbiter.

- Frame CRC Calculation
  - Useful for verification during production using pre-calculated checksums
  - CRC calculation of output frame (ST)
  - Result checking against reference value
  - Polynomial: CRC-CCITT (16 Bit)

CDC-500 Extensions

- Output Image Rotation
  - $90^o/270^o$ (optional: 180^o) image rotation
  - Rotation of post-layer-blending image
    - All layer features of all configured layers are available without functionality trade-offs
  - Resource-saving implementation
    - Only small internal FPGA/ASIC memory needed for rotation buffer

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CDC Family Overview

Feature	CDC-200	CDC-300	CDC-400	CDC-500
Layer Blending	×	×	×	×
Windowing	×	×	×	×
Gamma Correction	×	×	×	×
Color Keying	×	×	×	×
Dithering	×	×	×	×
Layer CLUT	×	×	×	×
RGB/Greyscale Input Formats	×	×	×	×
RGB888 Output	×	×	×	×
Dual View		×	×	×
Scaling		×	×	×
Mirroring (H & V)		×	×	×
YC_BC_R Input Formats		×	×	×
YC_BC_R Output Formats			×	×
Layer Blending Order			×	×
Missed-Pixel Handling			×	×
Single Frame Mode			×	×
Dual CPU Support			×	×
Frame CRC			×	×
Rotation				×

All features are configurable at synthesis time to implement only the functionality that is required in the target application.
For example, a customer who only needs YC_BC_R output formats, but no blend ordering, dual view and scaling, may order a **CDC-400** with these features disabled.
Even the **CDC-200** with its basic feature set may be configured to disable some of these features to reduce gate (ASIC) or logical element (FPGA) count and power consumption.

Power

- Memory blocks controlled by chip select port
- Clock gating of disabled layers logic + during blanking times
- Prepared for efficient automatic clock gating

Easy SoC Integration

- Low resource consumption
- Simple triple clock domain architecture
    - Slave bus clock, master bus clock and pixel clock are fully asynchronous
- High bus latency capable (pixel FIFO depth and number of outstanding reads configurable)
- Single bus master port (internal arbitration)
- Adaptors for common bus protocols

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- ARM AMBA: APB for register access,
  AHB or AXI4 for memory bus master access
- Altera Avalon as bus adaptors for both register and bus master access
- Other bus protocols can be easily adapted

Hardware Configuration Support

Comprehensive VHDL configuration package for:

- Configuration of layers
- Configuration of input pixel formats
- Enabling and disabling of certain features at synthesis time
- Configuration of register reset values
- etc.

Footprint

The footprint (FPGA logic cells or ASIC gate count) strongly depends on the configuration of the **CDC**. The number of layers, scaling and YC_BC_R support are the main factors influencing the resulting footprint.

A minimal **CDC-200** configuration (**CDC**, 1 layer, no YC_BC_R support, no scaling) starts at about 1000 ALMs (measured on an IntelPSG Arria10 FPGA) and between 15k-20k ASIC gates.

Software Drivers

TES provides a simple basic driver for register agnostic control of the **CDC**.

On top of the basic driver, a Khronos standard OpenWF Display API driver is available.

The drivers feature the following characteristics:

- Plain ANSI-C Code
- Fully reentrant & thread-safe
- Minimal OS dependency (HAL part separated), also runs on bare-metal
- No floating point usage
- No inline assembler required
- Small memory footprint

Drivers for other APIs can be developed on request.

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