Overview

The D/AVE HD GPU family is an evolution of the D/AVE 2D family supporting high quality 2D rendering and fixed function 3D rendering for displays up to 4K x 4K. Targeting modern graphics applications on high resolution displays in the Industrial, Medical, Military, Avionics, Automotive and Consumer markets, **D/AVE HD** is designed to be fast with powerful functionality. In addition, it is configurable and optimizable regarding size and footprint. The footprint optimized variants are the ideal choice e.g. for feature rich wearables, smart watches and IoT devices with animated 2D and 3D GUIs, while the fully featured variants target performance demanding graphics in professional and high-end consumer electronics applications.

D/AVE HD is available for both FPGA and ASIC integration with high customizability and scalability and already silicon proven e.g. in automotive products.

D/AVE HD configuration examples

The following table shows the feature-related D/AVE HD configuration options and presents some example configurations:

D/AVE HD	Example configurations			
GPU Variant / **Features**	**D/AVE HD-2.5D**	**D/AVE HD-3D**	**D/AVE HD-OVG**	**D/AVE HD-2.5D "Wearables"**
Technology	2D/3D Vector Graphics and advanced BLIT/transformation Engine			
Typical Application area	GUIs and 3D graphics on low-power MCUs and MPUs with no or simple OS (e.g. FreeRTOS)		Advanced MCUs and MPUs with simple or POSIX compliant OS (e.g. Linux)	Wearables
Highlight	HD resolution 2D/3D GUIs	+ advanced GUIs (perspective, true 3D depth buffer)	+ Full OpenVG / SVG HW support	2.5D
Gate count estimate	~230 k Gates	~300 k Gates	~450 k Gates	~330 k Gates
Memory size estimate (for 64bit AXI bus)	~67 k Bits	~120 k Bits	~120 k Bits	~67 k Bits
Target resolution	up to 4Mpix			
Peak performance	1 pixel/cycle			
Image compositing / blending	built-in	built-in	built-in	built-in
Image scaling / rotation (with filtering)	built-in	built-in	built-in	built-in
Subpixel precision, antialiasing	built-in	built-in	built-in	built-in
Complex linedrawing, triangle/rectangle drawing	built-in	built-in	built-in	built-in
Image warping (supported by Texture Swizzeling and Virtual Tiling)	built-in	built-in	built-in	built-in
Virtual tiling: Support to work efficiently with video source textures	built-in	built-in	built-in	built-in
Multi-threading support for multiple concurrent applications	built-in	built-in	built-in	built-in
3 dither modes including advanced stable dithering	built-in	built-in	built-in	built-in
FB compression to 1Bpp (without alpha) or 2Bpp (with alpha)	built-in	built-in	built-in	built-in
Per pixel min/max operators	built-in	built-in	built-in	built-in
RLE on-the-fly texture decompression	yes	yes	yes	yes
BC1 on-the-fly texture decompression	yes	yes	yes	yes
24bit texture and framebuffer formats	yes	yes	yes	yes
Advanced blending (porter duff, pre multiply/ post divide)	-	yes	yes	yes
True perspective texture mapping	-	yes	yes	yes
Multi texture units / per pixel lighting capabilities	1	2	2	1
Color transformation steps per pass	2	3	3	2
Full depth/stencil buffer support	-	yes	yes	-
Full OpenVG support	-	-	yes	-
Advanced vector rendering (native bezier curve support)	-	-	yes	yes
Arbitary image convolution (e.g. blur / sharpen)	-	-	yes	yes

Technology Details

Rendering

- High render quality
  - General sub pixel positioning
  - Direct-edge anti-aliasing
  - Blurring of primitive edges
- Hardware accelerated primitives
  - Fast clear/rectangle fill
  - (Poly-)Lines
  - Triangles
  - Quadrangles
  - Beziers (depending on variant)
  - Advanced Blit operations supporting scaling, stretching, rotating, coloring and alpha blending
  - Convolution Filtering (depending on variant)
- Fill styles
  - Constant color
  - Gouraud Shading (Alpha/Color Gradients)
  - Pattern
  - Multi-Texturing with perspective correction (depending on configuration)
- Blending
  - Normal alpha blending
  - Independent alpha/color blending
  - Source/Destination factors: 0, 1, source alpha, 1-source alpha
  - Advanced Blending modes : Porter-Duff, premultiply, postdivide (depending on configuration)
- Dithering: 3 dither-formats including TES stable dither-formats
  - TES stable “XOR”- and “Bayer_s” dithering: Applicable for all color formats with <8bit per channel, allowing “50% Framebuffer Compression” with high image quality by using standard RGB-565 format in combination with “Stable Dithering”. No framebuffer-decoder needed in this case.
- Various 8bit /16bit /24bit /32bit bitmap formats for textures and frame buffers
  - 8 bit alpha/luminance, ARGB4444, ARGB1555, RGB565, RGB888, ARGB8565, ARGB8888 ...
  - Indexed formats for CLUT (Color Look Up Table)
  - Easily extendable
- Frame buffers and textures up to 4k x 4k pixels
- Textures Compression Options:
  - Run-Length-Encoding (RLE) – lossless, compressed size depends on texture content
  - BC1-Compression – lossy, fixed compression rate of 4 bit per pixel (independent of content)
- Framebuffer Compression:
  - From ARGB8888 (4 Byte) to 1 Byte (without alpha) or 2 Byte (with Alpha) per Pixel
  - Requires TES CDC display controller with TES framebuffer-decompression
- Support for basic 3D graphics operations
  - Z-Buffer (depending on variant)
  - Texturing with perspective correction (depending on variant)
- Support for Image Transformation & Warping
- Rotation Engine
- Composition Engine

System Concept & Features

- Base version (single pipeline) 1 pixel per clock cycle (MPixels/s = MHz)
- Read prefetching / Multiple outstanding reads
  - No unnecessary reads (no full cache lines when not all pixels accessed)
  - Hide bus read latency
- Sophisticated caching mechanisms for command lists, textures and framebuffer data
- Optimization of applications by using detailed performance counters for
  - Total active cycles
  - Cache access efficiency
  - Bus accesses
  - etc.
- Pipelined architecture for high clock frequencies
- Hardware multi-threading support
  - Rendering jobs can be halted and resumed
  - Hardware can store and load rendering context
- System security features
  - Command list can be check-sum protected
  - Stop on bus error for integration with memory protection units
  - Hardware out-of-framebuffer memory access protection

Power

- Memory blocks controlled by Chip Select port
- Prepared for efficient automatic clock gating
- Global clock gating as option

Integration

- Low resource consumption (starting at 230K gates)
- Single clock domain architecture
- High latency capable
- All memories on top level
  - The memory signals from the D/AVE HD submodules are propagated to top level so that the memories can be instantiated either in the submodules or on top level
- 3-5 separate bus master interfaces vs. 1 single bus master (internal arbitration option)
- Adaptors for common bus protocols
  - ARM AMBA: APB for register access,
  - AHB or AXI (preferred) for memory bus master access
  - Other bus protocols can be easily adapted

Resource Usage

The actual resource usage of D/AVE HD depends mainly on the functional blocks coming with a configuration and partly on the bus and cache configuration. Please refer to the table above for typical gate counts.

Performance

The peak performance of 1 pixel per pixel pipeline can be achieved under the following conditions:
Large primitives

- Texture miss rate balanced compared to the available bus bandwidth
- Sufficient bus bandwidth in general
- The external bus architecture supports byte write enables (e.g. AXI) and sufficient internal buffers for handling outstanding accesses to hide the read latency

Memory read latencies for command list, texture and framebuffer read accesses can be hidden in principle with sufficient FIFO depth configuration in the prefetching caches.

Software Drivers

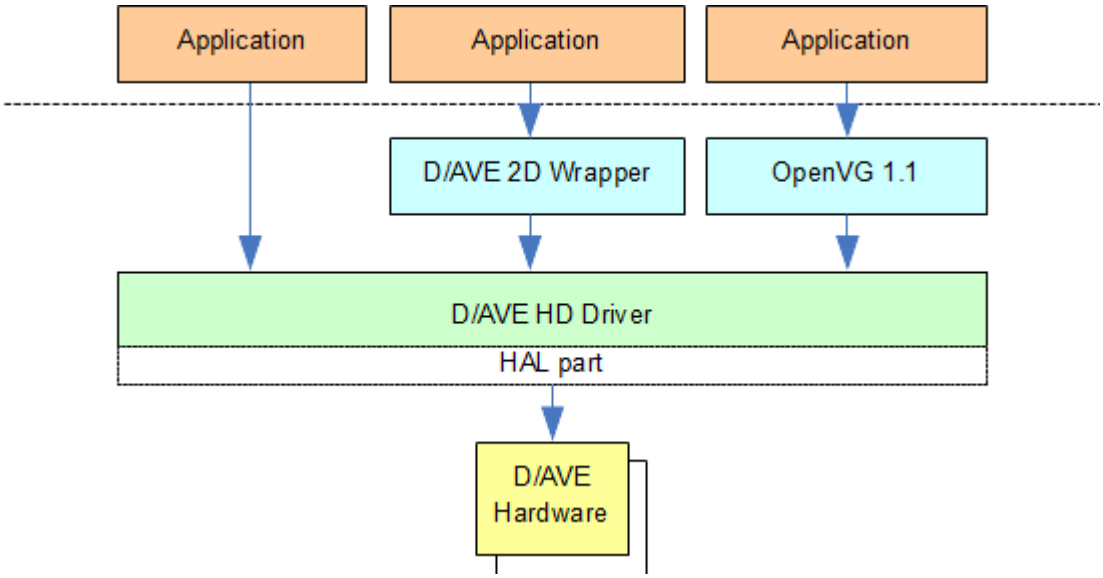
TES provides a Generic D/AVE HD API driver allowing easy usage of the high-level features of D/AVE HD without the need to directly access the registers. The driver is delivered for bare-metal, portings to other operation systems is possible on request.

The driver has the following features:

- Plain ANSI-C Code
- Fully reentrant & thread-safe
- Minimal OS dependency (HAL part separated) – allows easy porting
- No inline assembler required
- Support for multiple D/AVE HD instances
- Multi-threading support, i.e. multiple applications can use D/AVE HD concurrently, even via different APIs
- Small memory footprint

On top of this proprietary D/AVE HD API, standard APIs or Wrapper APIs can be provided on request:

- OpenVG 1.1
- D/AVE 2D Wrapper API
- Others are possible on request



Verification Concept

A 100% algorithmic equivalent C model is used as reference for the verification of the RTL code. This real-time capable reference model is called ‘SoftDave’ which acts as a pixel accurate emulator on Windows PC. The emulator is also used for driver and application development.

The following test metrics are used:
Functional Coverage

- Code Coverage using Cadence IUS
- Static Code Analysis
- Timing Checks
- FPGA prototyping

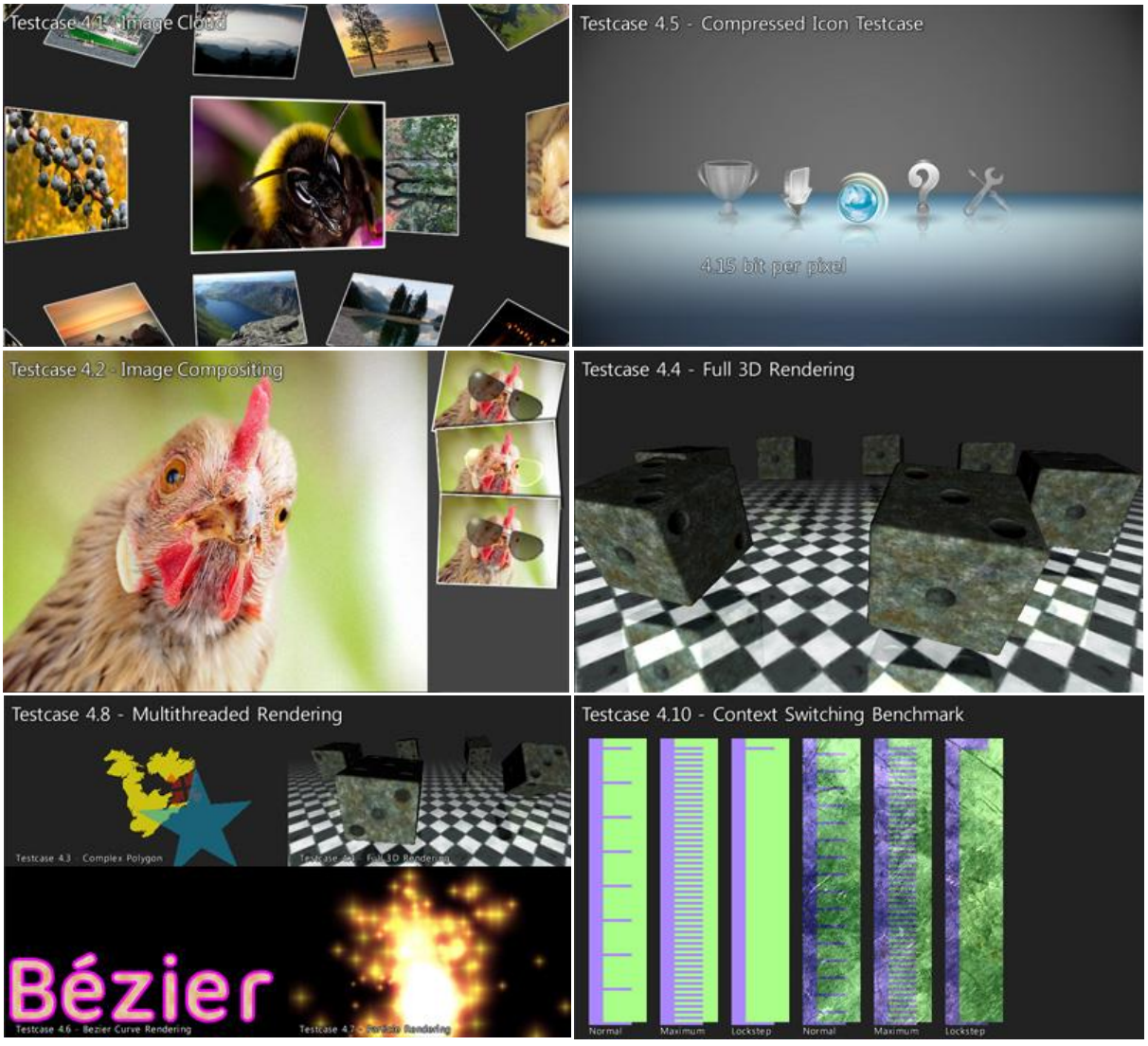
Evaluation Kits

Various options are available. All of them are delivered with:

- D/AVE HD bare metal drivers as precompiled library
- D/AVE HD demo and test applications as source code
- SoftDave: Pixel exact emulator for D/AVE HD allowing to run all provided applications on Windows PCs, i.e. no hardware is needed to take the first steps in evaluation D/AVE HD
- Installation guide, API documentation and tutorials

The SoftDave Evaluation Kit allows experiencing all D/AVE HD features without the need of any hardware beside a PC as well as the development of own graphics applications.

In addition, FPGA based Evaluation Kits can be offered allowing to experience D/AVE HD under real-time conditions and to integrate D/AVE HD with other IP cores for proof-of-concept and prototype purposes. They are either delivered with a ready to install FPGA image or (depending on the FPGA) a D/AVE HD Qsys component or encrypted VHDL code.



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