Overview

The D/AVE HD GPU family is an evolution of the D/AVE 2D family supporting high quality 2D rendering and fixed function 3D rendering for displays up to 4K x 4K. Targeting modern graphics applications on high resolution displays in the Industrial, Medical, Military, Avionics, Automotive and Consumer markets, **D/AVE HD** is designed to be fast with powerful functionality. In addition, it is configurable and optimizable regarding size and footprint. The footprint optimized variants are the ideal choice e.g. for feature rich wearables, smart watches and IoT devices with animated 2D and 3D GUIs, while the fully featured variants target performance demanding graphics in professional and high-end consumer electronics applications.
D/AVE HD is available for both FPGA and ASIC integration with high customizability and scalability and already silicon proven e.g. in automotive products.

D/AVE HD Linecard

The following standard variants of D/AVE HD are available. Customizations are possible based on customer request. Please feel free to contact us!

GPU Variant / Features	D/AVE HD-2.5D	D/AVE HD-3D	D/AVE HD-OVG	D/AVE HD-Dual
Technology	2D/3D Vector Graphics and advanced BLIT/transformation Engine			
Typical Application area	GUIs and 3D graphics on low-power MCUs and MPUs with no or simple OS (e.g. FreeRTOS)		Advanced MCUs and MPUs with simple or POSIX compliant OS (e.g. Linux)	
Highlight	HD resolution 2D/3D GUIs	+ advanced GUIs (perspective, true 3D depth	+ Full OpenVG / SVG HW support	+ High resolution dual pipeline processing
Footprint	~230 k Gates	~300 k Gates	~400 k Gates	~560k Gates
Target resolution	up to 4Mpix			up to 8Mpix
Peak performance	1 pixel/cycle			2 pixel/cycle
Image compositing / blending	yes	yes	yes	yes
Image scaling / rotation (with filtering)	yes	yes	yes	yes
Subpixel precision, antialiasing	yes	yes	yes	yes
Complex linedrawing, triangle/rectangle drawing	yes	yes	yes	yes
RLE on-the-fly texture decompression	yes	yes	yes	yes
4x to 20x performance for HD resolutions wrt. D/AVE 2D	yes	yes	yes	yes
Support to work efficiently with video source textures	yes	yes	yes	yes
Image warping	yes	yes	yes	yes
Multi-threading support for multiple concurrent applications	yes	yes	yes	yes
Advanced blending (porter duff, pre multiply/ post divide)	-	yes	yes	yes
True perspective texture mapping	-	yes	yes	yes
Multi texture / per pixel lighting capabilities	-	yes	yes	yes
Full depth/stencil buffer support	-	yes	yes	yes
Full OpenVG support	-	-	yes	yes
Advanced vector rendering (native bezier curve support)	-	-	yes	yes
Arbitary image convolution (e.g. blur / sharpen)	-	-	yes	yes
Advanced on-the-fly texture decompression	-	-	yes	yes
Efficient handling of large single channel (grayscale) data	-	-	-	yes
Combining more than two textures in one pass	-	-	-	yes
Per pixel min/max operators	-	-	-	yes
Additional color transformation	-	-	-	yes

Technology Details

Rendering

- High render quality
  - General sub pixel positioning
  - Direct-edge anti-aliasing
  - Blurring of primitive edges
- Hardware accelerated primitives
  - Fast clear/rectangle fill
  - (Poly-)Lines
  - Triangles
  - Quadrangles
  - Beziers (depending on variant)
  - Different connection styles for poly lines (useful e.g. for map applications): miter, round, bevel
  - Advanced Blit operations supporting scaling, stretching, rotating, coloring and alpha blending
  - Convolution Filtering (depending on variant)
- Fill styles
  - Constant color
  - Gouraud Shading (Alpha/Color Gradients)
  - Pattern
  - Multi-Texturing with perspective correction (depending on variant)
- Blending
  - Normal alpha blending
  - Independent alpha/color blending
  - Source/Destination factors: 0, 1, source alpha, 1-source alpha
- Various bitmap formats (textures and frame buffers)
  - 8 bit alpha/luminance, ARGB4444, ARGB1555, RGB565, ARGB8888 etc.
  - Indexed formats for CLUT (Color Look Up Table)
  - Easily extendable

Run-Length-Encoded Textures

- High resolutions

Frame buffers and textures up to 4k x 4k pixels

- Support for basic 3D graphics operations
  - Z-Buffer (depending on variant)
  - Texturing with perspective correction (depending on variant)
- Support for Image Transformation & Warping
- Rotation Engine
- Composition Engine

System Concept & Features

- Base version (single pipeline) 1 pixel per clock cycle (MPixels/s = MHz)
  - Core can scale to multiple parallel pixel pipelines to multiply pixel throughput
- Read prefetching / Multiple outstanding reads
  - No unnecessary reads (no full cache lines when not all pixels accessed)

    - Hide bus read latency
- Sophisticated caching mechanisms for command lists, textures and framebuffer data
- Optimization of applications by using detailed performance counters for
    - Total active cycles
    - Cache access efficiency
    - Bus accesses
    - etc.
- Pipelined architecture for high clock frequencies
- Hardware multi-threading support
    - Rendering jobs can be halted and resumed
    - Hardware can store and load rendering context
- System security features
    - Command list can be check-sum protected
    - Stop on bus error for integration with memory protection units
    - Hardware out-of-framebuffer memory access protection

Power

- Memory blocks controlled by Chip Select port
- Prepared for efficient automatic clock gating
- Global clock gating as option

Integration

- Low resource consumption (starting at 230K gates)
- Single clock domain architecture
    - Bus interface clock frequency may differ from core frequency
- High latency capable
- 3-5 separate bus master interfaces vs. 1 single bus master (internal arbitration option)
- Adaptors for common bus protocols
    - ARM AMBA: APB for register access,
    - AHB or AXI (preferred) for memory bus master access

Altera Avalon as bus adaptors for both register and bus master access
Other bus protocols can be easily adapted

Resource Usage

The actual resource usage of D/AVE HD depends mainly on the functional blocks coming with a variant, the number of pixel pipelines and partly on the bus and cache configuration. Please refer to the Linecard above for typical gate counts.

Performance

The peak performance of 1 pixel per pixel pipeline and cycle (2 pixel for D/AVE HD-Dual) can be achieved under the following conditions:
Large primitives

- Texture miss rate balanced compared to the available bus bandwidth
- Sufficient bus bandwidth in general
- The external bus architecture supports byte write enables (e.g. AXI) and sufficient internal buffers for handling outstanding accesses to hide the read latency

Memory read latencies for command list, texture and framebuffer read accesses can be hidden in principle with sufficient FIFO depth configuration in the prefetching caches.

Software Drivers

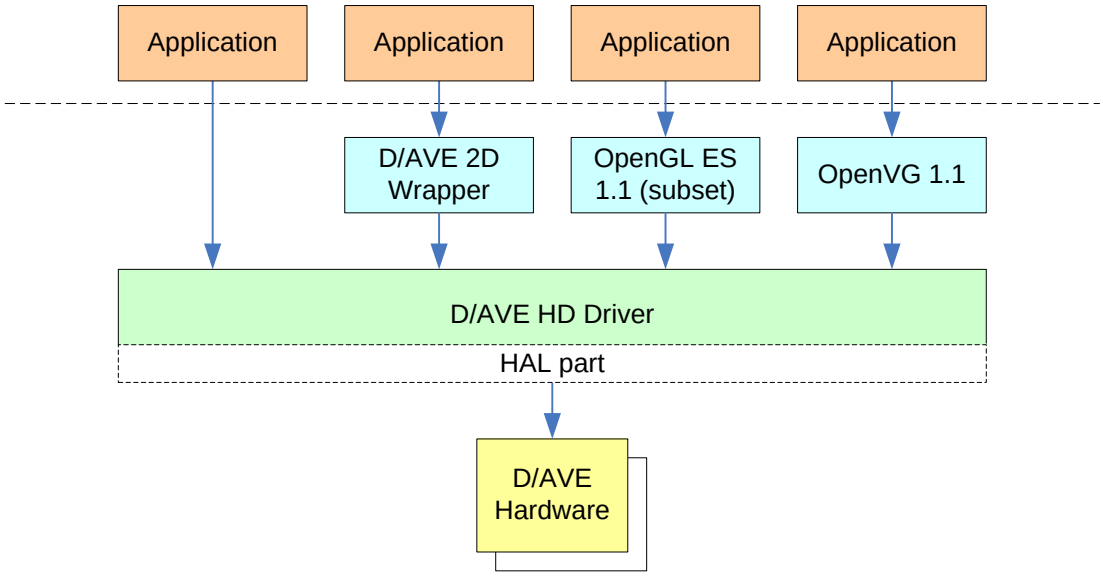
TES provides a Generic D/AVE HD API driver allowing easy usage of the high-level features of **D/AVE HD** without the need to directly access the registers.

The driver has the following features:

- Plain ANSI-C Code
- Fully reentrant & thread-safe
- Minimal OS dependency (HAL part separated)
- No floating-point usage
- No inline assembler required
- Support for multiple **D/AVE HD** instances
- Multi-threading support, i.e. multiple applications can use D/AVE HD concurrently, even via different APIs
- Small memory footprint

On top of this proprietary **D/AVE HD** API, standard APIs or Wrapper APIs can be provided on request:

- OpenVG 1.1
- OpenGL-ES 1.1 (subset)
- D/AVE 2D Wrapper API
- Others are possible



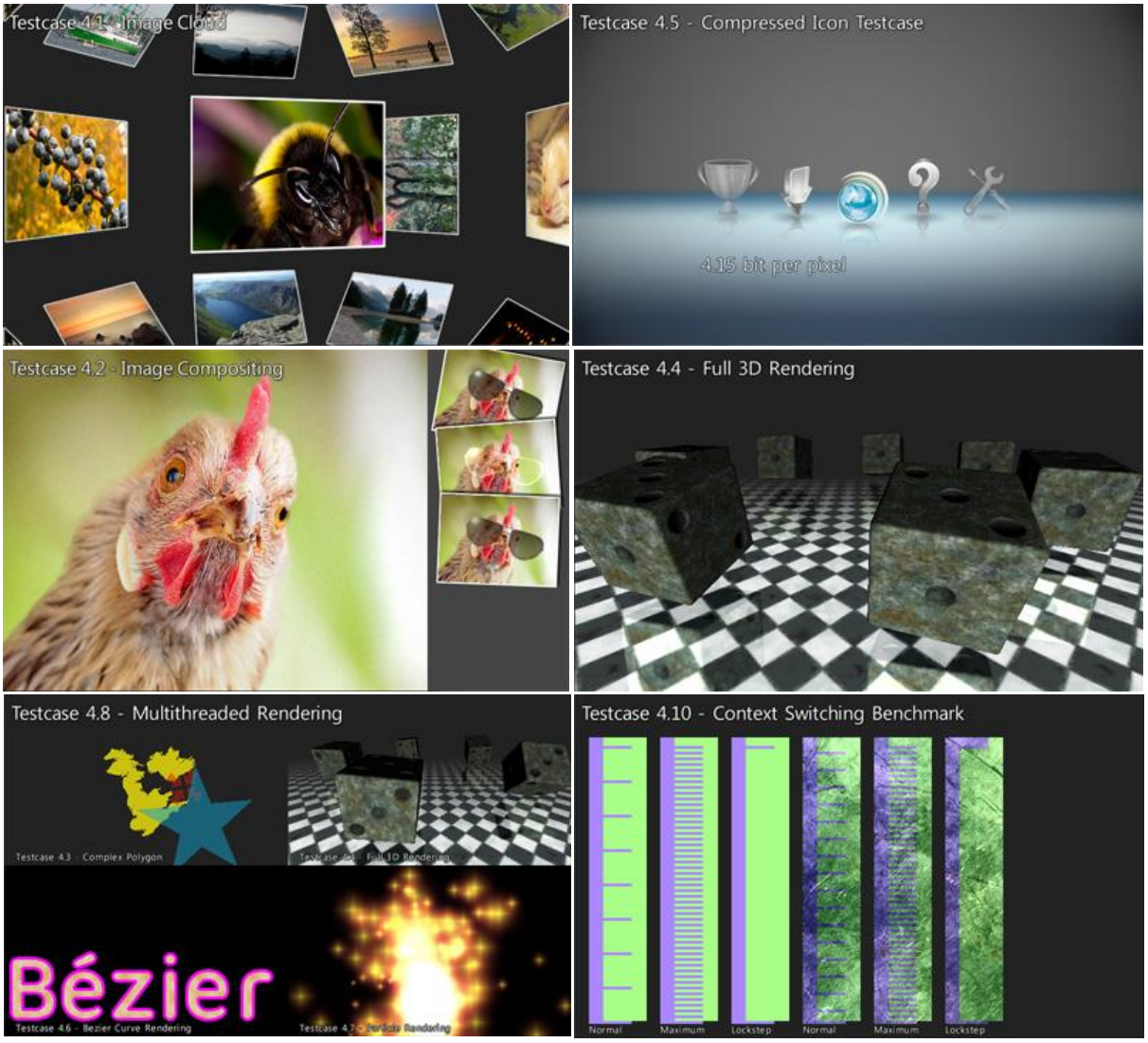
Evaluation Kit

D/AVE HD is delivered within an Evaluation Kit for Intel PSG FPGAs containing:

- Binary image files for selected FPGA boards
- D/AVE HD QSys component for the IntelPSG Quartus Toolchain with evaluation license
- D/AVE HD bare metal drivers as source code

- D/AVE HD demo and test applications as source code
- SoftD/AVE: Pixel exact emulator for D/AVE HD allowing to run all provided applications on Windows PCs, i.e. no hardware is needed to take the first steps in evaluation D/AVE HD
- Installation guide, API documentation and tutorials

Please contact us via **graphics@tes-dst.com** to obtain the evaluation kit!



Verification Concept

A 100% algorithmic equivalent C model is used as reference for the verification of the RTL code. This real-time capable reference model is called 'Soft D/AVE' which acts as a pixel accurate emulator on Windows PC. The emulator is also used for driver and application development.

The following test metrics are used:

Functional Coverage

- Code Coverage using Cadence IUS
- Static Code Analysis
- Timing Checks
- FPGA prototyping

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