

IP Data Sheet

Octuple 20µA Bias Current Source

The TS_CS_20uA_X8 is a current generator sourcing 20µA via each terminal IBPU<0> through IBPU<7>, for the biasing of other TES IPs like TS_FS_9M70_X8 and TS_VA_LNDC_X8 (for the latter IP, its input reference current must be mirrored from one Bias output by a simple cascoded NMOS circuit).

The Bias operates with two supply voltages, VDDA4 (4V typical) for its main function and VDDA5, VDDA5IO (5V typical) for the test-bus (ATB) circuit. It requires one precision reference voltage VREF (2.5V).

Precision current trimming is achieved under control

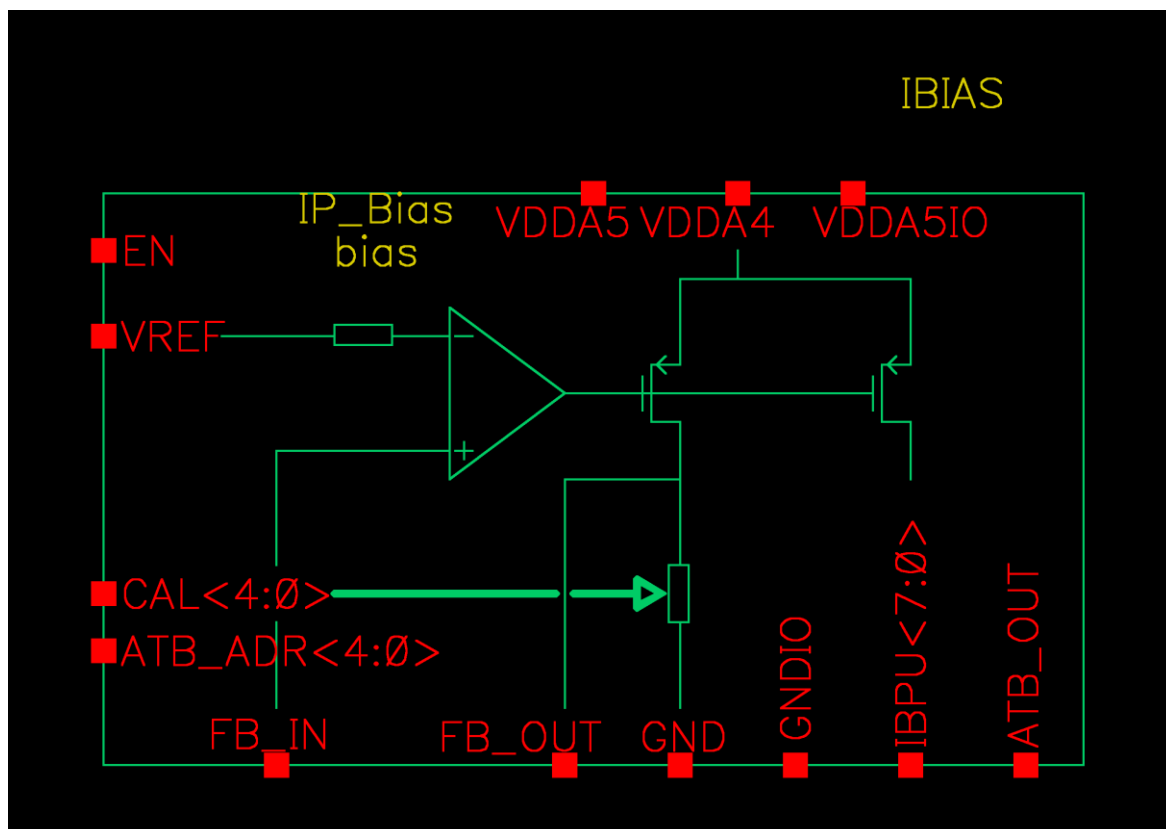
of the 5-bit calibration input CAL<4:0>.

This IP supports analog-test-bus multiplexing on the ATB_OUT output under control of the 5-bit address input ATB_ADR<4:0>. When ATB_ADR<4:0>= LLLHH, the Bias sources a 20µA current replica to ATB_OUT for off-chip measurement.

This IP complies with 2kV electrostatic discharges on its analog terminal ATB_OUT.

The minimum continuous operation lifetime spans 100000 hours.

Technology: X-FAB XT018-0.18µm BCD-on-SOI CMOS



Operating conditions

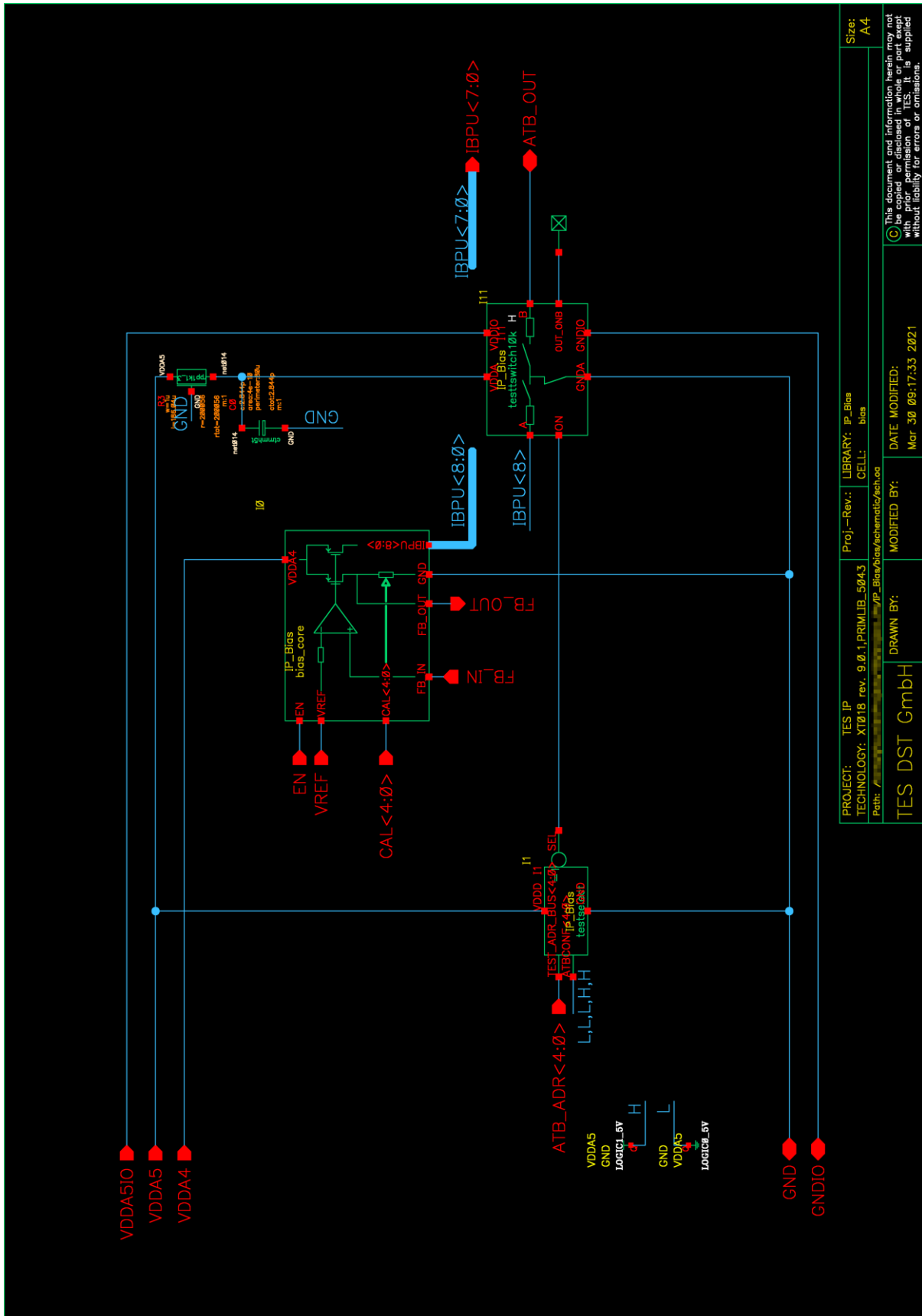
Parameters	Values
Junction temperature range	20°C to +80°C
Supply voltages	VDDA5, VDDA5IO: 4.9V to 5.1V VDDA4: 3.9V to 4.1V (supplied by the additional IP TS_VR_4V00_X8)
Reference voltage	VREF: 2.5V
Voltage at IBPU<7:0> terminals	2V max
EN, CAL<4:0> logic-high voltage level	VDDA4
ATB_ADR<4:0> logic-high voltage level	VDDA5

Specification

Parameters	Values
Calibrated output bias current intensity per IPBU output	20.0µA±0.5µA
Start-up time	2µs max
PSRR over frequencies from DC up to 10 MHz	5%/V max
Operating power consumption with unused IBPU<7:0>	765µW max
Powerdown-mode current consumption Enable EN low	11nA max
Area	0.031mm ²

FB_IN and FB_OUT must be interconnected.

BLOCK DIAGRAM



PROJECT: TES IP	Proj.-Rev.: LIBRARY: IP_Bias	Size: A4
TECHNOLOGY: XT018 rev. 9.0.1,PRIMLIB_5043	CELL: bias	
Path: /.../IP_Bias/bias/Achematic/Arch.co	MODIFIED BY: DATE MODIFIED: Mar_30_09:17:33_2021	
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LAYOUT VIEW

