IP Data Sheet

Clock Buffer

The TS_CLKBUF_25pF_X8 transfers input clock signal to other digital or mixed-signal chips, which feature altogether a maximum load capacitance of 25pF.

The clock buffer keeps the output voltage rise and fall times within the range of 1.4ns to 3.1ns over the load capacitance range of 1pF to 26pF. This minimizes the electromagnetic emission spectrum owing to output voltage slew rate.

The TS_CLKBUF_25pF_X8 works with a supply voltage of 3.3V, and features an enable signal. It consumes an average current of 6.5mA for a 40MHz input clock with the maximum load capacitance of 25pF. It has a typical propagation delay of 6ns for the maximum load.

The TS_CLKBUF_25pF_X8 can be used together with the TES IP crystal oscillator TS_XOSC_40M_X8 to generate and transfer a 8MHz / 40MHz clock signal to external chips.

Technology: X-FAB XT018-0.18µm BCD-on-SOI CMOS

OPERATING CONDITIONS

Parameters	Values
Junction temperature range	-40°C to 150°C
Supply voltage	3.2V to 3.4V
Square-wave input frequency	8MHz or 40MHz
Output load capacitance	25pF max

Table 1: Clock Buffer Operating Conditions

SPECIFICATION

Parameters	Values
Supply peak current intensity, CL = 1pF – 26pF	22.2mA to 112.2mA
Supply quiescent current intensity	172nA max
Output voltage rise / fall time, rising from 10% of supply to 90% of supply and vice versa, CL = 1pF – 26pF	1.4ns to 3.1ns

Table 2: Clock Buffer Specifications

LAYOUT VIEW

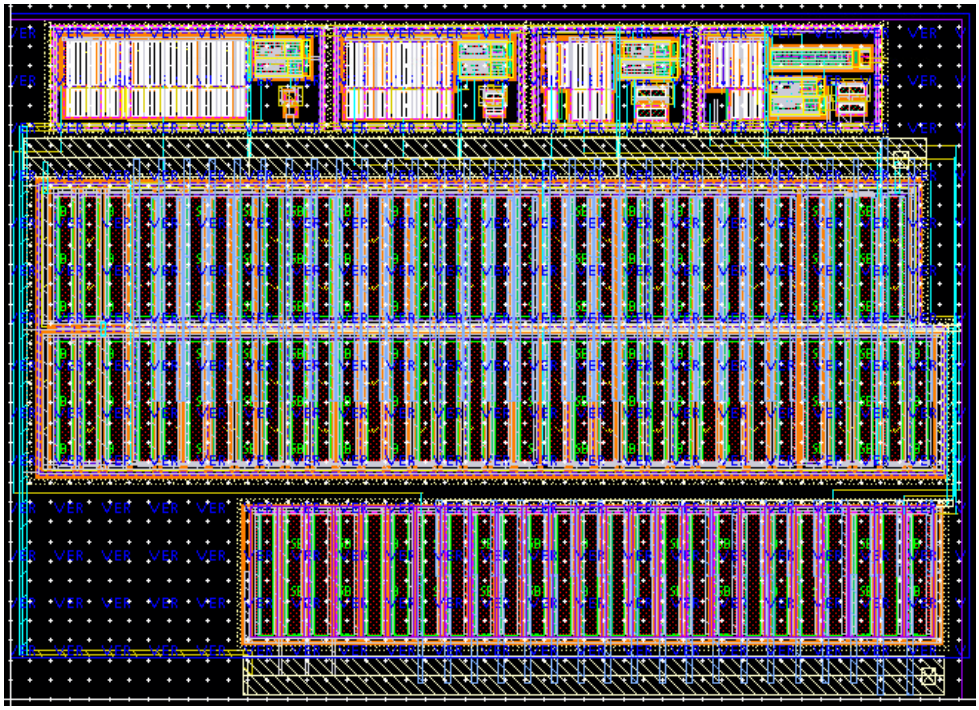

Figure 1: Layout View of the Clock Buffer

Sales & Marketing Contact

info@tes-dst.com