

IP Data Sheet

Integer-N-PLL-based HF Frequency Synthesizer and Clock Generator with integrated Loop Filter and VCO

This integer-N PLL synthesizes 3.3V-square-wave FVCO frequencies within the HF range from 2.424MHz up to 9.697MHz, by steps of 18.9393kHz, and provides one fourth of f_{VCO} on two other outputs, FDEM and FDRV, which feature quadrature phase difference or no phase shift depending on the control bit PH_SEL.

The PLL-locked state within $\pm 0.08\%$ of f_{VCO} is signaled by a logic high level on the LOCK output.

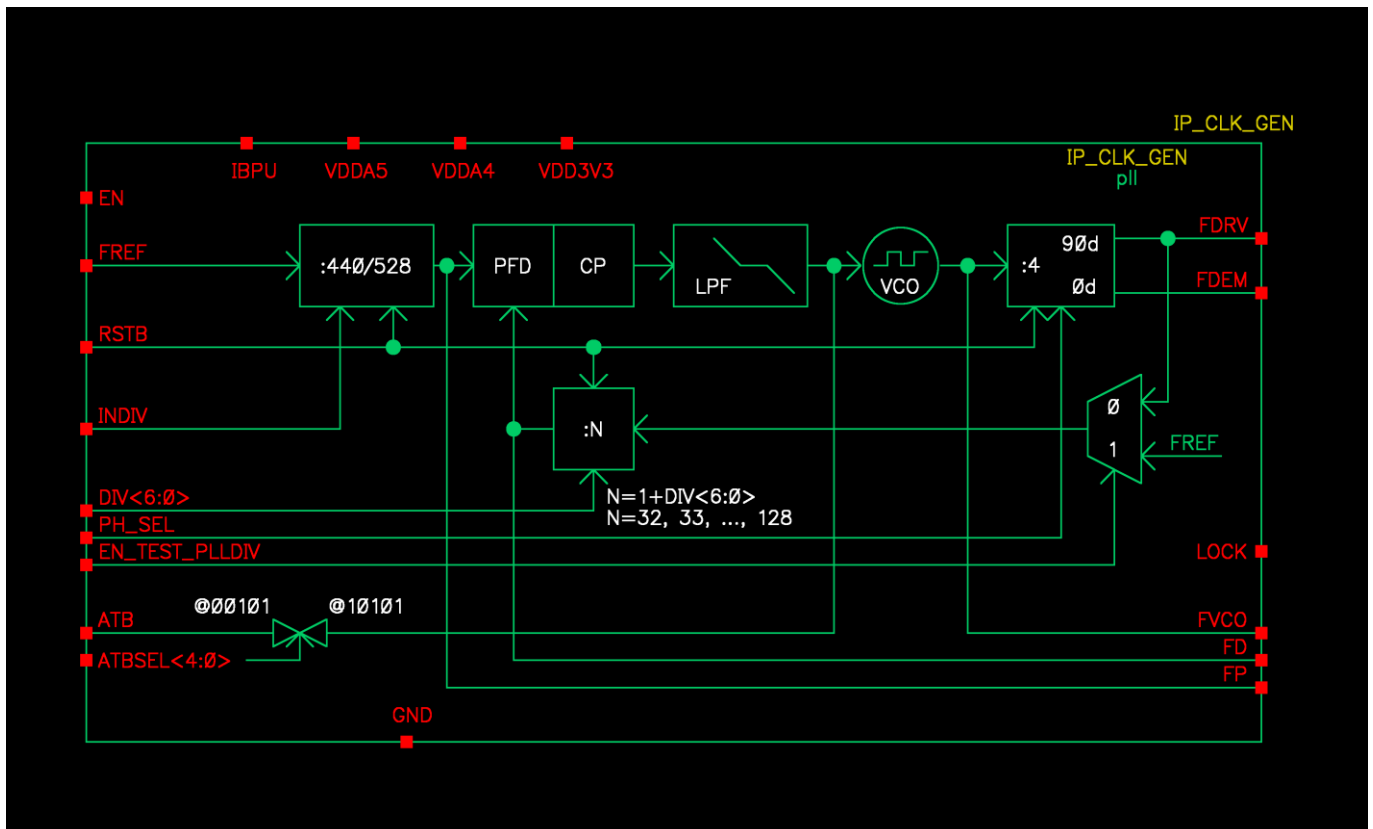
The PLL operates with three supply voltages, VDDA5 (5V typical), VDDA4 (4V typical from the additional IP TS_VR_4V00_X8) for the analog and test-bus

(ATB) circuits and VDD3V3 (3.3V typical from the additional IP TS_VR_3V30_X8) for the digital circuits.

The PLL is meant for on-chip internal operation. Its inputs or outputs that need access to bond pads will require the insertion of ESD-protected buffers. The ATB path complies with 2kV electrostatic discharges.

The minimum continuous operation lifetime spans 100000 hours.

Technology: X-FAB XT018-0.18 μ m BCD-on-SOI CMOS



Operating conditions

Parameters	Values
Junction temperature range	20°C to +80°C
Supply voltages	VDDA5: 4.9V to 5.1V VDDA4: 3.9V to 4.1V (supplied by the additional IP Reg_4V) VDD3V3: 3.2V to 3.4V (supplied by the additional IP Reg_3V3)
Reference sourced current intensity	I(IBPU): 19.5µA to 20.5µA (supplied by the additional IP Bias)
FREF-input reference frequency	8.333MHz or 10.000MHz

Specification

Parameters	Values
FVCO-output frequency range	2.424MHz to 9.697MHz
FVCO frequency step size	18.9393kHz
FDRV-/FDEM-output frequency range	606.06kHz to 2.424MHz
FVCO period jitter @2.424MHz	271p _{S_{RMS}} max
PLL lock time upon power on	4.95ms max
LOCK response time to PLL-locked state	150ms max
Operating power consumption Enable EN high, active-low reset RSTB high	870µW max
Powerdown-mode current consumption Enable EN low	187nA max
Area	0.16mm ²

DETAILED DESCRIPTION

This integer-N PLL synthesizes FVCO frequencies within the HF range from 2.424MHz up to 9.697MHz, from the reference clock applied to FREF:

$$f_{VCO} = 4 \times \frac{N_{FB}}{N_{IN}} \times f_{REF}$$

where N_{FB} is the division ratio of the feedback divider, pll_divider_7bit, with $N_{FB} = 1 + DIV(6:0)$,

and where N_{IN} is the division ratio of the reference divider, pll_prescaler, with two selectable-through-INDIV predefined N_{IN} values, 440 for INDIV = L and 528 for INDIV = H.

The synthesizer also provides one fourth of f_{VCO} on two other outputs, FDEM and FDRV, which feature quadrature phase difference when the control bit PH_SEL is set to L, and no phase shift otherwise.

The PLL loop bandwidth is a fraction of the PFD comparison frequency at 18.9393kHz (f_{FP} , reference divider output frequency, also f_{FD} , feedback divider output frequency). It is a function of the PLL natural frequency, while the loop filter pole and zero frequencies, as well as the PFD charge pump current intensity, are invariable by design.

$$PLL \text{ natural frequency} = \sqrt{\frac{K_{PDCP} \times K_{VCO}}{T \times 8\pi \times N_{FB}}}$$

K_{PDCP} : combined PFD/charge-pump/filter-capacitor slope obtained by integration over one PFD comparison period T ,

$$K_{PDCP} = \frac{I_{CP} \times T}{(C_1 + C_2) \times 2\pi}$$

K_{PDCP} =54.71mV/rad nominally, with charge-pump current intensity I_{CP} =312.5nA, $T = 1/f_{FP} = 52.8\mu s$ and C_1 =16pF, C_2 =32pF

$$K_{VCO} = 8\text{MHz/V}$$

For N_{FB} =128, PLL loop bandwidth = 3.746kHz.

For N_{FB} =32, PLL loop bandwidth = 7.385kHz.

The loop filter pole frequency, f_p , is placed at $(1 + \frac{C_2}{C_1}) = 3$ times the filter zero frequency,

$$f_z = \frac{1}{2\pi \times R_2 \times C_2} = 622\text{Hz}, \text{ with } R_2=8\text{M}\Omega. f_p=1865\text{Hz}.$$

The pole-zero disposition brings about a stability phase margin that tops out at 30.36° by 1.2kHz, and that exceeds the half for frequencies ranging from 261Hz up to 4.68kHz.

For N_{FB} =128, PLL stability phase margin = 22.58° at 2.532kHz,

For N_{FB} =32, PLL stability phase margin = 12.43° at 5.425kHz.

pll_lockdetector sets LOCK to H when f_{FD} equals f_{FP} within $\pm 2/2425 \times 100\%$. It signals for instance that f_{VCO} has reached the programmed frequency of 9.697MHz within $\pm 8\text{kHz}$.

The PLL can be put in three optional test modes:

- forced clocking of pll_divider_7bit by FREF when EN_TEST_PLLDIV is set to H,
- forced VCO control through an external voltage applied to ATB when ATBSEL<4:0>=LLHLH,
- VCO control voltage reading when ATBSEL<4:0>=HLHLH, and provided that a 100kΩ pulldown resistor is connected to ATB.

LAYOUT VIEW

