IP Data Sheet

Voltage Latched Comparator

A high-speed voltage clocked comparator with rail-to-rail outputs and no hysteresis. The typical propagation delay is 19ns while applying a differential input signal of 1mV over the offset voltage. The comparator operates with a supply voltage of 3.3V typical (VCC). The valid input voltage range is between 0.6V up to VCC. The comparator achieves an input offset voltage of ±1.04mV (3-sigma value). The circuit features an Enable signal turning on/off the comparator.

The comparator uses positive feedback (latch) to increase the comparison speed; thus, its operation consists of a reset phase and a regeneration (comparison) phase, which are controlled by the input clock (CLK). When CLK is 'High', the comparator is in the reset phase, and when it is 'Low', the comparator compares the voltages at INM and INP inputs and produces a 0 or VCC-level digital output voltage at the outputs DOUT and DOUTB. The CLK frequency is 2MHz. An output latch ensures that DOUT and DOUTB retain their previous values during reset phase.

The comparator features zero static current and low kickback noise. It requires a bias current of 89uA supplied from an external biasing circuit via the TAILBIAS input.

Technology: X-FAB XT018-0.18µm BCD-on-SOI CMOS

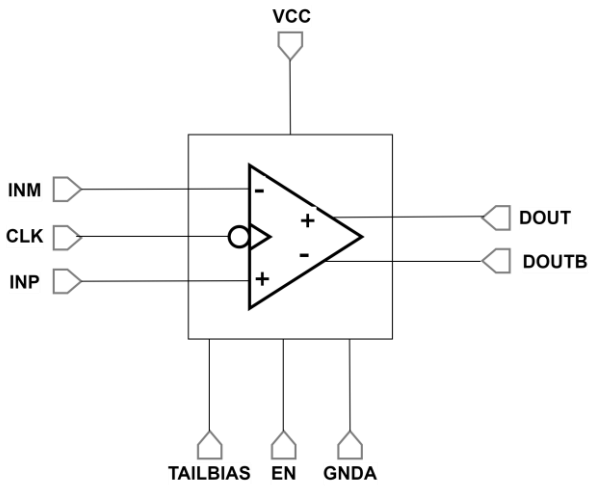

Figure 1: Voltage latched comparator symbol

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OPERATING CONDITIONS

Parameters	Min.	Typ.	Max.	Unit
Junction temperature range	-40	27	150	°C
Supply voltage on VCC with respect to ground GNDS	3.2	3.3	3.4	V

Table 1: Latched Comparator Operating Conditions

SPECIFICATION

Parameters	Condition	Min.	Typ.	Max.	Unit
propagation delay (low to high / high to low)	EN = H, V_{in_diff} = 1mV, C_L=100fF, V_{in_cm} = 1.25V	14.4	19.0	25.4	ns
Input offset voltage (V_{OS}) (3-sigma)	EN = H	-1.04		1.04	mV
Comparator Area			0.0043		mm^2

Table 2: Latched Comparator Specification

LAYOUT VIEW

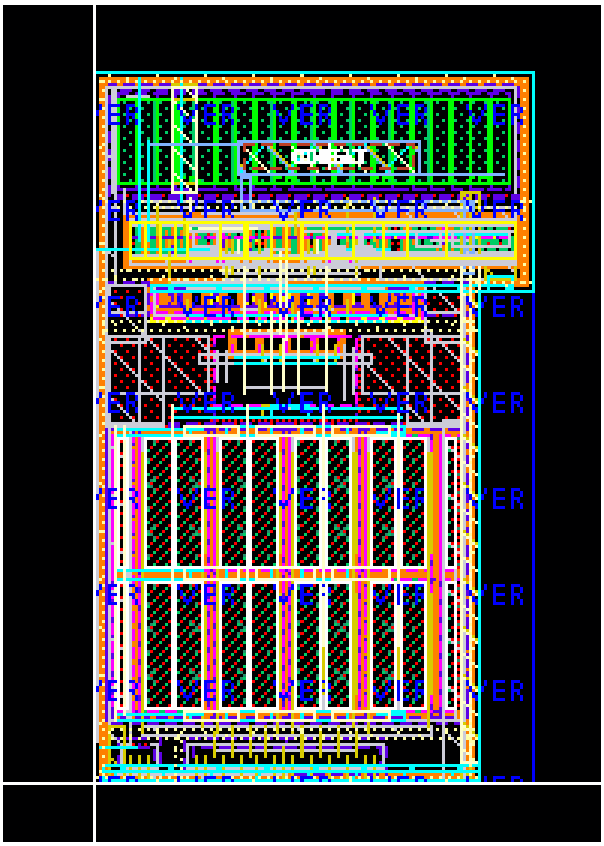

Figure 2: Voltage latched comparator layout